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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/830,117	TSAI ET AL.	
	Examiner	Art Unit	
	RuiMeng Hu	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,16-33,35-49,51-68,70-87 and 89-92* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,16-33,35-49,51-68,70-87 and 89-92* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on 10/22/2008 have been fully considered but they are not persuasive.

Regarding **Claim 39** that is rejected under 35 U.S.C. 102(e) as being anticipated by **Douziech et al. (US Patent 6781474).** Applicants argue that Douziech et al. fail to teach or suggest Applicants' claimed steps of generating a comparator output, generating a component code, and varying a gain based on the comparator output.

The Examiner respectfully submits that Douziech et al. disclose claim 39 in figures 1 and 4, calibrating the filter 11 based on the correction value outputted from the comparator 16, the correction value directly causes increment or decrement of the tuning voltage signal 27 by an amount of the correction value, thus the relationship between the correction value and the amount of frequency tuning in the filter is logical, further the correction value is unique each time to determine the amount of frequency tuning in the filter, thus the unique correction value functions as a code. Thus Douziech et al. disclose steps of generating a comparator 16 output, generating a component code (a unique voltage code), and varying a gain based on the comparator output (figure 4, varying an amplifier based on the comparator 16 output).

Regarding **Claims 1, 20 and 39** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kluge et al. (US Patent 7184729)** in view of **Gabara (US Patent 6307443).** Applicants argue that there is no reasonable rationale for incorporating Gabara's variable amplifier into Kluge's automatic gain control circuit.

The Examiner respectfully submits that claim 1 fails to mention adjusting the filter circuit based on the comparator output, thus the filter adjusting means and the amplifier varying means are two different and independent process means. Kluge et al. disclose in figure 1a, an automatic gain control circuit comprising: tunable filter circuit 110 passes a received RF signal. Gabara discloses figure 1 and the Abstract, the Abstract recites: "the tuning signal is adjusted until the passed power is maximized, indicating that the filter is tuned to the dominant frequency." A tunable bandpass filter 12 is tuned to the dominant frequency of the received signal for a maximum gain. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection techniques taught by Gabara into the art of Kluge et al. as to include the filter calibration circuit comprising devices 12, 20, 34 and 36 to tune the frequency of the filter circuit to the dominant frequency for precisely selecting the received signal and maximizing the received signal gain, in addition to the automatic gain control of Kluge et al.

Same argument applies to claim 20.

Consider **claim 39**, The Examiner respectfully submits that Kluge et al. disclose A method for calibrating a filter circuit (figure 1a), the filter circuit 110 receiving an input signal and producing a filtered output signal, the method comprising: generating a comparator 130 output based on a filter output amplitude signal and a reference amplitude signal (figure 1a, Reference voltages), the filter output amplitude signal corresponding to an amplitude of the filtered output signal at a desired frequency (figure 1a, filter 110 at a received frequency); generating a component code (152) based on the

comparator 130 output; adjusting one or more component values in the filter circuit 110 based on the component code 152; producing a fixed DC reference amplitude signal (Reference voltages); and varying a gain (varying a gain of filter circuit 110) based on the comparator 130 output.

Regarding **Claims 1-14, 16-33, 35-38, 55-68, 70-87 and 89-92** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Johnson (US Patent 6766150 B1)** in view of **Miyazaki (US Patent 5081713).** Applicants argue that there is no reasonable rationale for incorporating Miyazaki's reference voltage generator and variable gain high frequency amplifier circuit into Johnson's filter calibration circuit.

The Examiner respectfully submits that claim 1 fails to mention adjusting the filter circuit based on the comparator output, thus the filter adjusting means and the amplifier varying means are two different and independent process means. Johnson discloses a RF transmitter in figure 3, a filter calibration circuit comprising tunable filter 345 and filter calibration controller 365, and a variable gain amplifier 330. However, Johnson fails to disclose a DC voltage source operable to produce the reference amplitude signal; a variable gain amplifier, the calibration logic unit operable to vary a gain of the variable gain amplifier based on the comparator output. Miyazaki discloses a RF transmitter in figures 1 and 2, an automatic gain control circuit comprising: detector 16 for detecting signal level of an power amplified RF output signal, a DC voltage source 27 operable to produce the reference amplitude signal; a variable gain amplifier and amplifier gain control circuit (figure 2) wherein the variable gain amplifier 11 is controlled by a power controller 18 based on the comparison result (output of comparator 17) of a reference

voltage (output of 27) and a feedback detected power level (output of 16). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection techniques taught by Miyazaki into the art of Johnson as to add the automatic gain control circuit showed in figure 1 or 2, to adjust amplifier 330 to amplify the output signal to wanted reference level therefore enhancing reception quality in a corresponding receiver.

Same argument applies to claims 20, 55 and 74.

Regarding claims 3, 8, 43 and 45, The Examiner respectfully submits that the teaching of LC tank filter is well known in the art, wherein a component code (voltage) varies a capacitance in the filter circuit, as disclosed by Rice et al. (US Patent 5917387) (column 3 lines 6-35, figure 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection techniques taught by Rice et al. into the art of Johnson as modified as to use the LC filter as an alternative embodiment.

Regarding claims 16 and 51, The Examiner respectfully submits that the limitation is inherently disclosed when a user power on the transmitter and starts communication.

Regarding claims 17 and 52, The Examiner respectfully submits that the filter calibration circuit of Johnson is operable to calibrate the filter circuit within its capacity.

Regarding **Claim 39** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Johnson (US Patent 6766150 B1)** in view of **Gabara (US Patent 6307443).** Applicants argue that there is no reasonable rationale to combine Gabara and Johnson.

The Examiner respectfully submits that Johnson discloses in column 7 lines 37-42, producing a fixed DC reference amplitude signal (the pre-determined reference voltage V_REF), and in column 9 lines 34-43 a fixed reference amplitude signal (values of signal levels stored within internal software of filter calibration controller 365).

In the same field of endeavor, Gabara discloses a filter tuning circuit comprising producing a fixed DC reference amplitude signal and a DC value can be digitized and stored in a DSP (column 1 lines 26-49, column 2 lines 4-15).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection techniques taught by Gabara into the art of Johnson as to produce, digitize and store fixed DC reference amplitude signals in a DSP, in which the stored DC reference amplitude signals are set equal to the values of signal levels stored within internal software, thus establishes a hardware version of the filter calibration circuit carried out by a DSP wherein the DSP is common in a wireless radio frequency terminal.

Response to Amendment

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claim 39** is rejected under 35 U.S.C. 102(e) as being anticipated by **Douziech et al. (US Patent 6781474).**

Consider **claim 39**, Douziech et al. disclose A method for calibrating a filter circuit (figures 1 and 4), the filter circuit receiving an input signal and producing a filtered output signal, the method comprising: generating a comparator 16 output based on a filter output amplitude signal and a reference amplitude signal (figure 1, values 21 and 22 are references to each other, or figure 4, Vref), the filter output amplitude signal corresponding to an amplitude of the filtered output signal at a desired frequency (figure 1, feedback output signal to level detector 13); generating a component code (output of comparator 16) based on the comparator 16 output; adjusting one or more component values in the filter circuit 11 based on the component code; producing a fixed DC reference amplitude signal (figure 4, Vref); and varying a gain (figure 4, a variable amplifier) based on the comparator 16 output.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1, 20 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kluge et al. (US Patent 7184729)** in view of **Gabara (US Patent 6307443).**

Consider **claim 1**, Kluge et al. clearly disclose a filter calibration circuit (figures 1a, 1b), comprising: a comparator 130 operable to generate a comparator output based on a filter output amplitude signal and a reference amplitude signal 133, the filter output amplitude signal corresponding to an amplitude of an output signal produced by a filter circuit 107,108; and a calibration logic unit 140,150 operable to receive the comparator output and produce a component code 103 to be used by the filter circuit 107,108 in

adjusting one or more component values in the filter circuit 107,108; a DC voltage source operable to produce the reference amplitude signal 133; a variable gain amplifier 105, the calibration logic unit 140,150 operable to vary a gain of the variable gain amplifier 105 based on the comparator 130 output.

However Kluge et al. fail to disclose the filter circuit that is to be calibrated to a desired frequency.

Gabara discloses a filter frequency tuning circuit for tuning a filter to a desired frequency (figure 1, Abstract).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection techniques taught by Gabara into the art of Kluge et al. as to tune the filter circuit to the desired center frequency for enhancing output signal.

Consider **claims 20 and 39,** see response to **claim 1** above**.**

Claims 1-14, 16-33, 35-38, 55-68, 70-87 and 89-92 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Johnson (US Patent 6766150 B1)** in view of **Miyazaki (US Patent 5081713).**

Consider **claim 1**, Johnson clearly discloses a filter calibration circuit (figure 3, column 9 lines 34-65), comprising: a comparator 365 operable to generate a comparator output based on a filter output amplitude signal and a reference amplitude signal, the filter output amplitude signal corresponding to an amplitude of an output signal produced by a filter circuit 345 that is to be calibrated to a desired frequency

(column 9 lines 34-65); and a calibration logic unit 365 operable to receive the comparator output and produce a component code (365 outputs digital code control signal) to be used by the filter circuit 345 in adjusting one or more component values in the filter circuit 345; and the stored reference amplitude signal (column 9 lines 34-65).

However Johnson fails to disclose a DC voltage source operable to produce the reference amplitude signal; a variable gain amplifier, the calibration logic unit operable to vary a gain of the variable gain amplifier based on the comparator output.

In the same field of endeavor, Miyazaki clearly discloses a DC voltage source 27 operable to produce the reference amplitude signal; a variable gain amplifier and amplifier gain control circuit (figure 2) wherein the variable gain amplifier 11 is controlled by a power controller 18 based on the comparison result (output of comparator 17) of a reference voltage (output of 27) and a feedback detected power level (output of 16).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection techniques taught by Miyazaki into the art of Johnson as to include a DC voltage source to produce the reference amplitude signal as an alternative embodiment; and to adjust amplifier 330 to amplify the output signal to a desired level based on the comparator output, specially for the case when the output signal level is still below the desired level even after the filter is adjusted to center frequency.

Consider **claim 20**, see response to claim 1.

Consider **claim 2 as applied to claim 1**, **claim 21 as applied to claim 20, claim 40 as applied to claim 39**, Johnson as modified clearly discloses further comprising: an

amplitude detector (figure 3, detector 365) operable to receive the filter circuit output signal and generate the filter output amplitude signal based on an amplitude of the filter circuit output signal at the desired frequency (figure 3, column 9 lines 34-65).

Consider **claim 3 as applied to claim 1**, **claim 22 as applied to claim 20,** Johnson as modified fail to disclose wherein: the filter circuit includes an LC tank circuit. Official Notice is taken that the teaching is well known in the art. Therefore, the LC tank filter circuit is tuned to the center frequency.

Consider **claim 4 as applied to claim 1, claim 23 as applied to claim 20**, Johnson as modified clearly discloses wherein: the calibration logic unit includes a digital signal processor 365.

Consider **claim 5 as applied to claim 4**, **claim 24 as applied to claim 23**, Johnson as modified clearly discloses wherein: the digital signal processor includes the comparator (unit 365 compares).

Consider **claim 6 as applied to claim 1**, **claim 25 as applied to claim 20**, Johnson as modified clearly discloses wherein: the calibration logic unit includes a logic circuit (figure 3, column 9 lines 34-65).

Consider **claim 7 as applied to claim 6**, **claim 26 as applied to claim 25**, Johnson as modified clearly discloses wherein: the logic circuit includes the comparator (unit 365 compares).

Consider **claim 8 as applied to claim 1**, **claim 27 as applied to claim 20**, Johnson as modified clearly discloses wherein: the component code varies a capacitance in the filter circuit (consider tuning a LC tank filter).

Consider **claim 9 as applied to claim 8**, **claim 28 as applied to claim 27**, Johnson as modified clearly discloses wherein: the capacitance varied is monolithically fabricated on a semiconductor substrate (365 can be integrated on a semiconductor substrate).

Consider **claim 10 as applied to claim 8**, **claim 29 as applied to claim 27**, Johnson as modified clearly discloses wherein: the component code varies the capacitance by controlling a number of capacitive elements active in the filter circuit (consider tuning a LC tank filter).

Consider **claim 11 as applied to claim 1**, **claim 30 as applied to claim 20**, Johnson as modified clearly discloses further comprising: a digital-to-analog converter operable to receive a digital reference amplitude code and produce the reference amplitude signal (figure 3, column 9 lines 34-65).

Consider **claim 12 as applied to claim 11**, **claim 31 as applied to claim 30**, Johnson as modified clearly discloses wherein: the calibration logic unit is operable to produce the digital reference amplitude code based on the comparator output (figure 3, column 9 lines 34-65).

Consider **claim 13 as applied to claim 1**, **claim 32 as applied to claim 20**, Johnson as modified clearly discloses further comprising: an analog-to-digital converter operable to receive the filter output amplitude signal and produce a corresponding digital amplitude code (figure 3, column 9 lines 34-65).

Consider **claim 14 as applied to claim 13**, **claim 33 as applied to claim 32**, Johnson as modified clearly discloses wherein: the comparator is operable to use the

digital amplitude code as the filter output amplitude signal and a stored digital amplitude code as the reference amplitude signal (figure 3, column 9 lines 34-65).

Consider **claim 16 as applied to claim 1**, **claim 35 as applied to claim 20,** Johnson as modified clearly discloses wherein: the filter calibration circuit is operable to calibrate the filter circuit to the desired frequency automatically when the filter calibration circuit is connected to a power source (figure 3, column 9 lines 34-65).

Consider **claim 17 as applied to claim 1**, **claim 36 as applied to claim 20,** Johnson as modified clearly discloses wherein: the filter calibration circuit is operable to calibrate the filter circuit to the desired frequency without requiring a reduction in a quality factor of the filter circuit (figure 3, column 9 lines 34-65).

Consider **claim 18 as applied to claim 1**, **claim 37 as applied to claim 20,** Johnson as modified clearly discloses wherein: the filter calibration circuit is operable to calibrate the filter circuit to the desired frequency without requiring manual calibration of the filter circuit (figure 3, column 9 lines 34-65).

Consider **claim 19 as applied to claim 1**, **claim 38 as applied to claim 20,** Johnson as modified fails to disclose wherein: the filter calibration circuit is compliant with any of IEEE standards 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, 802.11i, 802.11n, and 802.16.

Official Notice is taken that the teaching of a filter calibration circuit, which is compliant with IEEE standards, is well known in the art; therefore, a person skilled in the art would easily incorporate this teaching as to increase the functionality.

Consider **claim 55**, Johnson clearly discloses a wireless transceiver (figure 3, column 9 lines 34-65), comprising: a transmitter operable to transmit a modulated carrier signal, the transmitter including a filter circuit 345 operable to filter the modulated carrier signal and a calibration circuit 365 operable to calibrate the filter circuit to a desired frequency, the calibration circuit including, a comparator 365 operable to generate a comparator output based on a filter output amplitude signal and a reference amplitude signal (column 9 lines 34-65), the filter output amplitude signal corresponding to an amplitude of an output signal produced by the filter circuit 345; a calibration logic unit 365 (365 outputs digital code control signal) operable to receive the comparator output and produce a component code to be used by the filter circuit 345 in adjusting one or more component values in the filter circuit 345, and the stored reference amplitude signal (column 9 lines 34-65).

However Johnson fail to disclose a DC voltage source operable to produce the reference amplitude signal; and a variable-gain amplifier, the calibration logic unit operable to vary a gain of the variable- gain amplifier based on the comparator output.

In the same field of endeavor, Miyazaki clearly discloses a DC voltage source 27 operable to produce the reference amplitude signal; a variable gain amplifier and amplifier gain control circuit (figure 2) wherein the variable gain amplifier 11 is controlled by a power controller 18 based on the comparison result (output of comparator 17) of a reference voltage (output of 27) and a feedback detected power level (output of 16).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection techniques taught by

Miyazaki into the art of Johnson as to include a DC voltage source to produce the reference amplitude signal as an alternative embodiment; and to adjust amplifier 330 to amplify the output signal to a desired level based on the comparator output, specially for the case when the output signal level is still below the desired level even after the filter is adjusted to center frequency.

Consider **claim 74**, see response to **claim 55** above.

Consider **claim 56 as applied to claim 55**, **claim 75 as applied to claim 74,** Johnson as modified clearly discloses wherein the calibration circuit includes: an amplitude detector (detector 365) operable to receive the filter circuit 345 output signal and generate the filter output amplitude signal based on an amplitude of the filter circuit output signal at the desired frequency (figure 3, column 9 lines 34-65).

Consider **claim 57 as applied to claim 55**, **claim 76 as applied to claim 74,** Johnson as modified fail to disclose wherein: the filter circuit includes an LC tank circuit. Official Notice is taken that the teaching is well known in the art. Therefore, the LC tank filter circuit is tuned to the center frequency.

Consider **claim 58 as applied to claim 55**, **claim 77 as applied to claim 74,** Johnson as modified clearly discloses wherein: the calibration logic unit includes a digital signal processor 365.

Consider **claim 59 as applied to claim 58**, **claim 78 as applied to claim 77,** Johnson as modified clearly discloses wherein: the digital signal processor includes the comparator (365 compares).

Consider **claim 60 as applied to claim 55**, **claim 79 as applied to claim 74,** Johnson as modified clearly discloses wherein: the calibration logic unit includes a logic circuit (figure 3, unit 365).

Consider **claim 61 as applied to claim 60**, **claim 80 as applied to claim 79,** Johnson as modified clearly discloses wherein: the logic circuit includes the comparator (365 compares).

Consider **claim 62 as applied to claim 55**, **claim 81 as applied to claim 74,** Johnson as modified clearly discloses wherein: the Component code varies a capacitance in the filter circuit (considering tuning LC tank filter).

Consider **claim 63 as applied to claim 62**, **claim 82 as applied to claim 81,** Johnson as modified clearly discloses wherein: the capacitance varied is monolithically fabricated on a semiconductor substrate (365 can be integrated on a semiconductor substrate).

Consider **claim 64 as applied to claim 62**, **claim 83 as applied to claim 81,** Johnson as modified clearly discloses wherein: the component code varies the capacitance by controlling a number of capacitive elements active in the filter circuit (consider tuning a LC tank filter).

Consider **claim 65 as applied to claim 55**, **claim 84 as applied to claim 74,** Johnson as modified clearly discloses wherein the calibration circuit includes: a digital-to-analog converter operable to receive a digital reference amplitude code and produce the reference amplitude signal (figure 3).

Consider **claim 66 as applied to claim 65**, **claim 85 as applied to claim 84,** Johnson as modified clearly discloses wherein: the calibration logic unit is operable to produce the digital reference amplitude code based on the comparator output (figure 3).

Consider **claim 67 as applied to claim 55**, **claim 86 as applied to claim 74,** Johnson as modified clearly discloses wherein the calibration circuit includes: an analog-to-digital converter operable to receive the filter output amplitude signal and produce a corresponding digital amplitude code (figure 3).

Consider **claim 68 as applied to claim 67**, **claim 87 as applied to claim 86,** Johnson as modified clearly discloses wherein: the comparator is operable to use the digital amplitude code as the filter output amplitude signal and a stored digital amplitude code as the reference amplitude signal (figure 3, column 9 lines 34-65).

Consider **claim 70 as applied to claim 55**, **claim 89 as applied to claim 74,** Johnson as modified clearly discloses wherein: the calibration circuit is operable to calibrate the filter circuit to the desired frequency automatically when the calibration circuit is connected to a power source (figure 3, column 9 lines 34-65).

Consider **claim 71 as applied to claim 55**, **claim 90 as applied to claim 74,** Johnson as modified clearly discloses wherein: the calibration circuit is operable to calibrate the filter circuit to the desired frequency without requiring a reduction in a quality factor of the filter circuit (figure 3, column 9 lines 34-65).

Consider **claim 72 as applied to claim 55**, **claim 91 as applied to claim 74,** Johnson as modified clearly discloses wherein: the calibration circuit is operable to

calibrate the filter circuit to the desired frequency without requiring manual calibration of the filter circuit (figure 3, column 9 lines 34-65).

Consider **claim 73 as applied to claim 55, claim 92 as applied to claim 74,** Johnson as modified fails to disclose wherein: the filter calibration circuit is compliant with any of IEEE standards 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, 802.11i, 802.11n, and 802.16.

Official Notice is taken that the teaching of a filter calibration circuit, which is compliant with IEEE standards, is well known in the art; therefore, a person skilled in the art would easily incorporate this teaching as to increase the functionality.

Claims 39-49 and 51-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Johnson (US Patent 6766150 B1)** in view of **Gabara (US Patent 6307443).**

Consider **claim 39**, Johnson clearly discloses a method for calibrating a filter circuit (figure 3, column 9 lines 34-65), the filter circuit 345 receiving an input signal and producing a filtered output signal (figure 3), the method comprising: generating a comparator output (365 compares) based on a filter output amplitude signal and a reference amplitude signal (stored reference signal level), the filter output amplitude signal corresponding to an amplitude of the filtered output signal at a desired frequency (figure 3, feedback signal); generating a component code (output of 365) based on the comparator output; and adjusting one or more component values in the filter circuit 345 based on the component code (figure 3, column 9 lines 34-65); and varying a gain

based on the comparator output (tuning the filter to center frequency to produce a maximum gain for the output signal).

However Johnson fails to disclose producing a fixed DC reference amplitude signal.

In the same field of endeavor, Gabara discloses a filter tuning circuit comprising producing a fixed DC reference amplitude signal (column 1 lines 26-49, column 2 lines 4-15).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the selection techniques taught by Gabara into the art of Johnson as to produce a fixed DC reference amplitude signal and store reference amplitude signal as an alternative embodiment.

Consider **claim 41 as applied to claim 39**, Johnson as modified clearly discloses wherein: generating the component code includes digitally generating the component code (figure 3, column 9 lines 34-65).

Consider **claim 42 as applied to claim 41**, Johnson as modified clearly discloses wherein: generating the comparator output includes digitally generating the comparator output (figure 3, column 9 lines 34-65).

Consider **claim 43 as applied to claim 39**, Johnson as modified clearly discloses wherein: adjusting one or more component values includes adjusting a capacitance in the filter circuit (consider tuning a LC tank filter, Gabara, column 1 lines 26-28).

Consider **claim 44 as applied to claim 43**, Johnson as modified clearly discloses wherein: adjusting a capacitance includes adjusting a capacitance monolithically fabricated on a semiconductor substrate (Gabara, column 1 lines 9-10, the filter is being fabricated as part of integrated circuits (semiconductor substrate)).

Consider **claim 45 as applied to claim 43**, Johnson as modified clearly discloses wherein: adjusting a capacitance includes controlling a number of capacitive elements active in the filter circuit (consider tuning a LC tank filter, Gabara, column 1 lines 26-28).

Consider **claim 46 as applied to claim 39**, Johnson as modified clearly discloses further comprising: producing the reference amplitude signal based on a digital reference amplitude code (Gabara, column 1 lines 26-45, DC reference voltage is stored on the DSP, column 3 lines 20-26, magnitude of the previous input is stored on the digital memory).

Consider **claim 47 as applied to claim 46**, Johnson as modified clearly discloses further comprising: producing the digital reference amplitude code based on the comparator output (figure 3, column 9 lines 34-65).

Consider **claim 48 as applied to claim 39**, Johnson as modified clearly discloses further comprising: producing a digital amplitude code based on the filter output amplitude signal (figure 3, column 9 lines 34-65).

Consider **claim 49 as applied to claim 48**, Johnson as modified clearly discloses further comprising: using the digital amplitude code as the filter output amplitude signal (figure 3, column 9 lines 34-65); and using a stored digital amplitude

code as the reference amplitude signal (figure 3, column 9 lines 34-65, Gabara, column 1 lines 26-45, DC reference voltage is stored on the DSP).

Consider **claim 51 as applied to claim 39,** Johnson as modified clearly discloses wherein: the filter calibration circuit is operable to calibrate the filter circuit to the desired frequency automatically when the filter calibration circuit is connected to a power source (figure 3, column 9 lines 34-65).

Consider **claim 52 as applied to claim 39,** Johnson as modified clearly discloses wherein: the filter calibration circuit is operable to calibrate the filter circuit to the desired frequency without requiring a reduction in a quality factor of the filter circuit (figure 3, column 9 lines 34-65).

Consider **claim 53 as applied to claim 39,** Johnson as modified clearly discloses wherein: the filter calibration circuit is operable to calibrate the filter circuit to the desired frequency without requiring manual calibration of the filter circuit (figure 3, column 9 lines 34-65).

Consider **claim 54 as applied to claim 39,** Johnson as modified fails to disclose wherein: the filter calibration circuit is compliant with any of IEEE standards 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, 802.11i, 802.11n, and 802.16.

Official Notice is taken that the teaching of a filter calibration circuit, which is compliant with IEEE standards, is well known in the art; therefore, a person skilled in the art would easily incorporate this teaching as to increase the functionality.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to:**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RuiMeng Hu whose telephone number is 571-270-1105. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lana Le can be reached on (571)272-7891. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/RuiMeng Hu/
R.H./rh
January 21, 2009

/Lana N. Le/

Primary Examiner, Art Unit 2614